AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A NAND flash memory cell row, comprising:

a substrate;

a plurality of first stacked gate structures disposed on the substrate, wherein each of the first stacked gate structures comprises an erase gate dielectric layer, an erase gate and a first cap layer;

two second stacked gate structures disposed on the substrate beside two outer sides of the first stacked gate structures respectively, wherein each of the second stacked gate structures comprises a select gate dielectric layer, a select gate and a second cap layer;

a plurality of control gates disposed between the first stacked gate structures and each of the second stacked gate structures, and between every two of the neighboring first stacked gate structures;

a plurality of floating gates disposed between the control gates and the substrate, wherein each of the floating gates has sharp corners and a concave surface facing each of the control gates, and the edge of the concave surface is lower than a top surface of the erase gate;

an inter-gate dielectric layer disposed between each of the control gates and each of the floating gates;

a tunnel oxide layer, disposed between each of the floating gates and the substrate, between each of the floating gates and the first stacked gate structures, and between each of the floating gates and the second stacked gate structures;

a plurality of doping regions disposed in the substrate under the first stacked gate structures; and

a plurality of source/drain regions disposed in the exposed substrate outside the second stacked gate structures.

2. (original) The NAND flash memory cell row of claim 1, wherein a material of the tunnel oxide layer comprises a silicon oxide.

3. (original) The NAND flash memory cell row of claim 1, wherein the inter-gate dielectric layer comprises a material selected from the group consisting of silicon oxide/silicon nitride/silicon oxide, silicon nitride/silicon oxide and silicon oxide/silicon nitride.

4. (original) The NAND flash memory cell row of claim 1, wherein the first and the second cap layers comprise an oxide layer and a dielectric layer disposed on the oxide layer.

5. (original) The NAND flash memory cell row of claim 1, wherein the NAND flash memory cell further comprising:

a p-type well region disposed in the substrate, wherein a depth of the p-type well region is deeper than a depth of the source/drain regions.

Claims 6-16 (canceled).